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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,500	07/08/2003	Matthew J. Adiletta	10559-075002 / P7567	8894
20985	7590	12/23/2005	EXAMINER	
FISH & RICHARDSON, PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			ELLIS, RICHARD L	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,500	ADILETTA ET AL.	
	Examiner Richard Ellis	Art Unit 2183	

~ The MAILING DATE of this communication appears on the cover sheet with the correspondence address ~

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 07 October 2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 36-41 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 36-41 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 20050628.
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

1. Claims 36-41 are newly presented for examination.
2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.
3. Claims 36-41 are rejected under 35 USC § 103 as being unpatentable over Hwang, U.S. patent 6,216,220 in view of Shaw et al., *Unix Internals, A systems Operations Handbook*, 1987.

Hwang taught (e.g. see figs. 1-6) the invention as claimed (as per new claim 36), including a data processing ("DP") system comprising:

- A. a processor chip (fig. 3) comprising;
- B. a reduced instruction set computer (RISC) core (4); and,
- C. multiple multi-threaded programmable units (2-1, 2-2, 2-3) communicatively coupled (3) with the reduced instruction set computer core (4), each of the multiple multi-threaded programmable (2-1, 2-2, 2-3) units comprising a control store ("REGISTER", "STATUS WORD") and storage for multiple program counters ("PROGRAM COUNTER") associated with the, respective, multiple threads (1).

Hwang is silent as to whether each of the multi-threaded programmable units contain logic to re-enable availability for execution of a one of multiple threads in response to a signal associated with a memory reference issued by the thread. Hwang does teach moving threads to a wait queue in response to a long latency event such as a memory reference (col. 4 lines 45-54). Hwang is silent as to how these threads are removed from this wait queue, which must happen, or else all threads will eventually be placed upon the wait queue and the processor will stop executing instructions due to there being no threads in the ready queue.

Shaw et al. taught that it was known that threads (processes) normally incur events that take a significant amount of time to complete (long latency) (pg. 30, only paragraph on page) and gives examples of certain kinds of long latency events (pg. 31, the text on the page). Shaw et al. further taught that when these events occur, the thread is put on a sleep queue (wait queue) (pg. 33, first paragraph on page). Shaw et al. further taught that when the long latency

event completes, the thread that is on the wait queue is moved back to the ready queue to await scheduling for execution (pg. 33, second paragraph on page).

4. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Shaw et al.'s teaching of moving threads from the wait queue to the ready queue when the long latency event the thread is waiting upon completes with Hwang's system because of Hwang's silence as to what to do with threads on the wait queue. Recognizing that once all threads are on the wait queue the system will cease to execute any programs, one of skill in the art would be motivated to look for other art which provided teachings of how and why processes move from the wait queue to the ready queue.
5. As to claim 37, Hwang did not teach that each of the multiple multi-threaded programmable units comprised a programmable unit having a multi-stage instruction pipeline. However, Hwang did suggest to modify the system to be multi-stage pipelined at (col. 7 lines 19-24). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Hwang such that the multiple multi-threaded programmable units comprised a multi-stage instruction pipeline because of Hwang suggestion to make such a change at col. 7 lines 19-24.
6. As to claims 40-41, they do not teach or define above the invention claimed in claims 36-37 and are therefore rejected under Hwang in view of Shaw et al. for the same reasons set forth in the rejection of claims 36-37, supra.
7. Claims 38-39 are rejected under 35 USC § 103 as being unpatentable over Hwang, in view of Shaw et al. as applied to claims 36-37 and 40-41, and further in view of Kaiserswerth, *The Parallel Protocol Engine*, IEEE 1993.

Hwang and Shaw et al. taught the invention substantially as detailed in the rejection of claims 36-37 and 40-41, supra. Hwang and Shaw et al. did not teach that the system was useful for performing network protocol data path operations.

Kaiserswerth taught that a multiple processor system was useful for performing network protocol data path operations (pg. 651, col. 1, lines 30-37). It would have been

obvious to a person of ordinary skill in the art at the time the invention was made to have utilized the system of Hwang and Shaw et al. as a network protocol data path processor because of Kaiserswerth's teachings that parallel processing systems allow for substantial speedups in processing of network protocol data units (pg. 651, section 2.1 through 2.3) Additionally, Kaiserswerth references Hwang's multi-program counter system as advantageous for implementing a network protocol processing system (pg. 655, col. 2, lines 39-49). Additionally, Kaiserswerth indicated that a software implementation was preferred (pg. 651, col. 1, line 39 to col. 2, line 4).

8. Applicant's arguments with respect to new claims 36-41 have been considered but are deemed to be moot in view of the new grounds of rejection.
9. Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a).

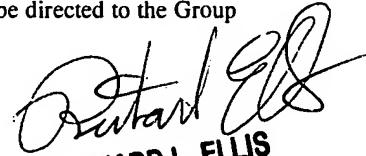
A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Richard Ellis
December 15, 2005



RICHARD L. ELLIS
PRIMARY EXAMINER